**THE UNIVERSITY OF DANANG**

**UNIVERSITY OF SCIENCE AND TECHNOLOGY**

**Faculty of Advanced Science and Technology**



**LABORATORY REPORT**

**INTRODUCTION TO VERY LARGE SCALE INTERGRATION IC DESIGN**

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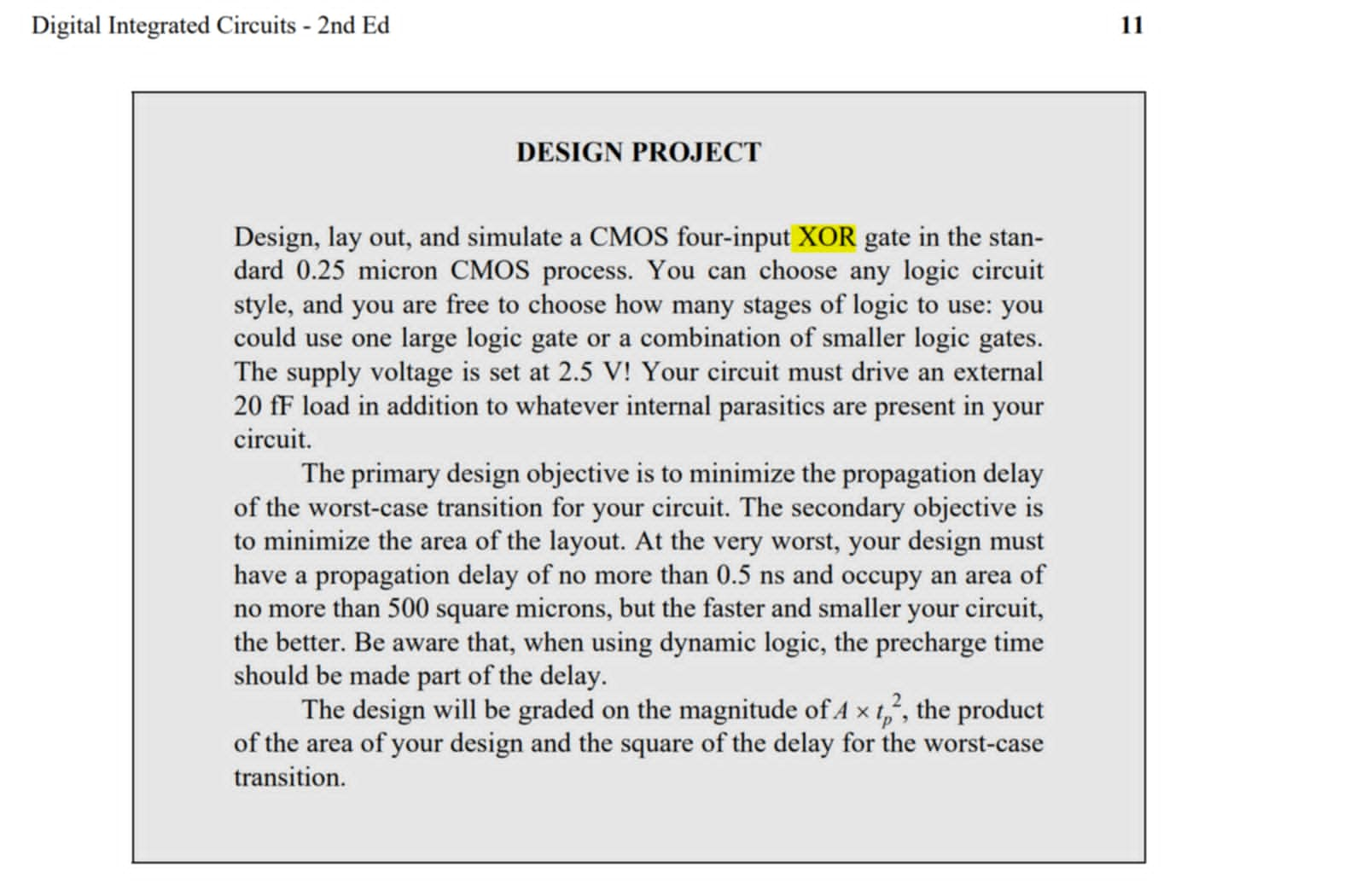
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# Technical Design

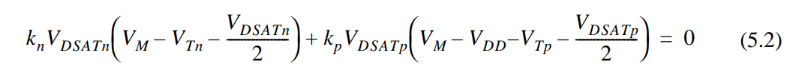
## Technical Objectives:

* Design a **4-input XOR gate** using CMOS technology with a **0.25-micron process**.
* Ensure that the circuit has a propagation delay of less than **0.5 ns**.
* The **circuit area** must not exceed **500 square microns**.
* The **supply voltage** is **2.5V**, and the circuit must drive an external load of **20 fF**.

## Performance Requirements:

* Check the propagation delay and optimize the transistor sizes to meet the required delay.
* Use simulation tools to measure the circuit's parameters.

## Design Technique:

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**VDD =2.5 (V) so**

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**A diagram of a circuit

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From the requirement with external load = 20 fF, so:

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For a supply voltage of 2.5 V, the normalized on-resistances of NMOS and PMOS transistors equal 13 kW and 31 kW, respectively. (table 3.3)

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* Reqn = 13kΩ; Reqp =31kΩ

* **We must choose to obtain tp < 0.5 ns**

And

* To have propagate delay < 5ns, the size of invertor must be:

Wp <14.03 um and Wn < 5.20 um

* **Choose:**

So, Cint of of reference invertor is:

# Physical Design:

## Design of the Transistor for a 2-input XOR Gate:

* A 2-input XOR gate can be constructed using 12 transistors (6 PMOS and 6 NMOS).
* Design the pull-up network with PMOS and the pull-down network with NMOS transistors.

## 2-input XOR Gate:

* PMOS in the pull-up network is activated when the input is low, pulling the output high.
* NMOS in the pull-down network is activated when the input is high, pulling the output low.

## Combining 2-input XOR Gates:

* To create a 4-input XOR gate, combine three 2-input XOR gates. Use a 3-stage XOR structure to calculate the output of the 4-input XOR:
  + Stage 1: Z1=A⊕B, Z2=C⊕D
  + Stage 2: Y=Z1⊕Z2 ​

A diagram of a circuit

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# Logic Design:

## Logic Equation for a 4-input XOR Gate:

Y=A ⊕ B ⊕ C ⊕ D

Or Y = (A⊕B) ⊕ (C⊕D)

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* Logic diagram:

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* Truth table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input** | | | | **Output** |
| **A** | **B** | **C** | **D** | **Y** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **1** | **0** | **1** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** | **1** |
| **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **0** |
| **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **0** |
| **1** | **0** | **1** | **1** | **1** |
| **1** | **1** | **0** | **0** | **0** |
| **1** | **1** | **0** | **1** | **1** |
| **1** | **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** | **0** |

## Logic circuit simulation:

* The logic signal is simulated by using tool DSCH .

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# Layout Design:

## Layout Creation Process:

* Physical layout of the circuit by using tool Microwind.

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* Check DRC (dessign rule check).

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**A computer screen shot of a computer program

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**A screenshot of a computer screen

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**A computer screen shot of a computer program

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**A screenshot of a video game

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# Conclusion

**Achieved Results**: Summarize the requirements and the outcomes of the design, such as the circuit area, propagation delay, and A×tp2A \times t\_p^2A×tp2​ value.

**Comments**: Provide comments on the achieved results, potential improvements, and practical applications of this 4-input XOR gate.